



WBS 6.3

Overview of US ATLAS

Liquid Argon (LAr) Calorimeter

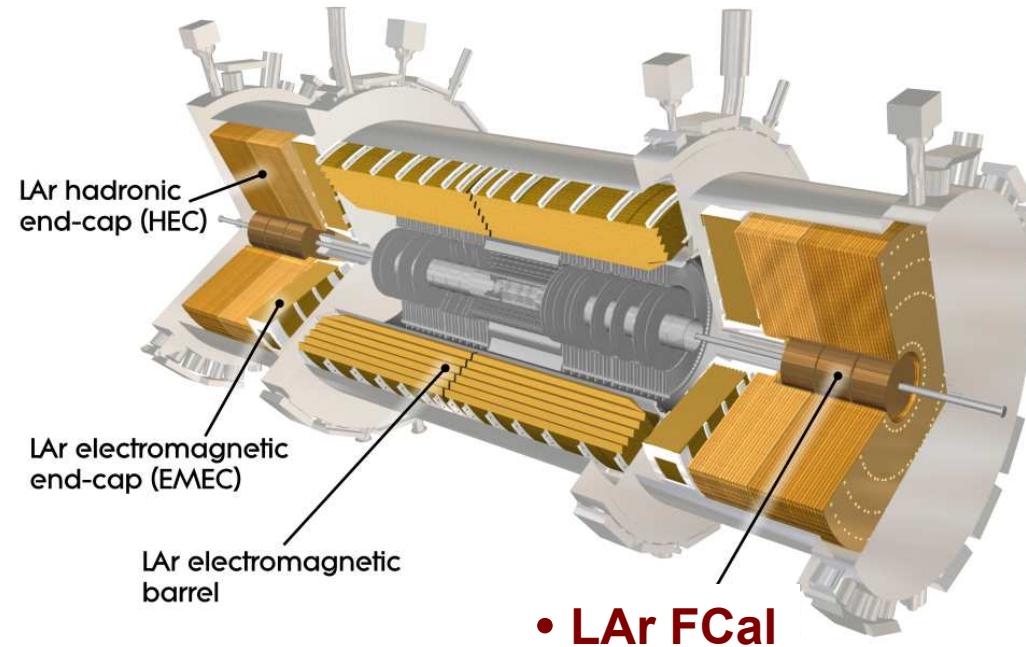
Phase II Upgrade Planning

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Columbia University

April 8, 2015

LAr Phase-II Upgrade Project

- Readout Electronics



ATLAS Phase II Upgrade:

Replace the LAr Calorimeter Electronics
and possibly the Forward Calorimeter (FCal)



FCAL



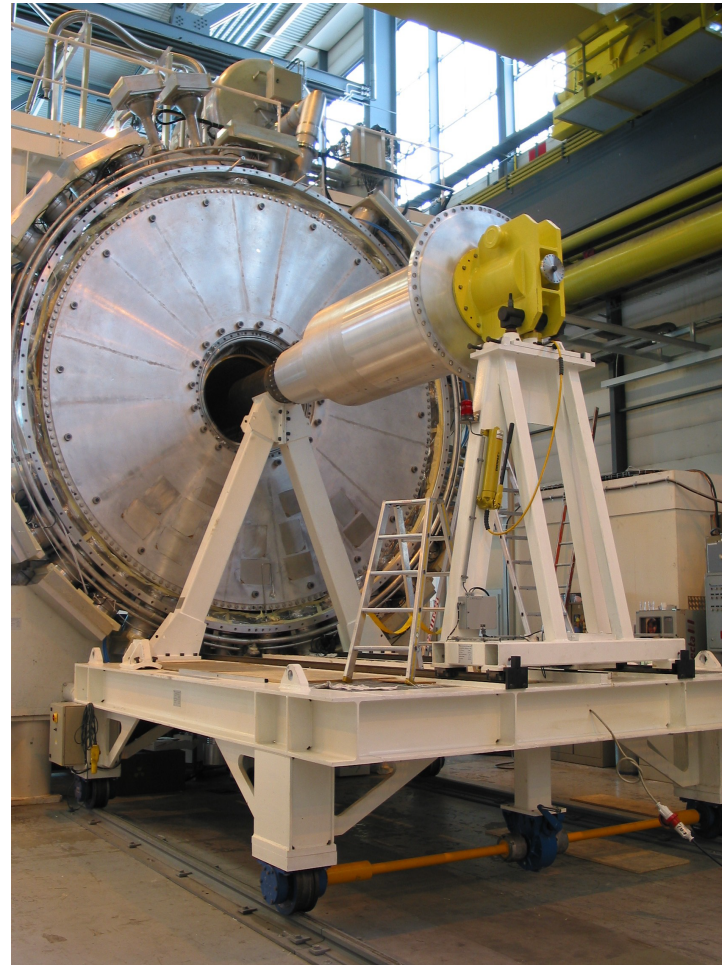
LAr Detector Options in Lol

- Option 0: No change neither of the HEC cold electronics nor of the FCal detectors.
- ~~● Option 1: If the HEC cold electronics have to be replaced (Sec. 3.2.2), the large cold cryostat cover would have to be opened and the irradiated FCal would have to be removed. A newly built cold FCal (sFCal) (Sec. 3.2.3) would then be inserted before closing the cryostat.~~
- Option 2: If the HEC cold electronics do not have to be replaced, the cold FCal would be replaced by a new one of the sFCal type (Sec. 3.2.3). It is anticipated that only the small cover of the cold vessel, the FCal bulkhead, would have to be removed.
- Option 3: If the HEC cold electronics do not have to be replaced, the cold FCal would stay in place and a new small calorimeter (Mini-FCal) (Sec. 3.2.4) would be placed in front of it. In this case only the cryostat warm vessel would have to be opened.



Endcap Cryostat

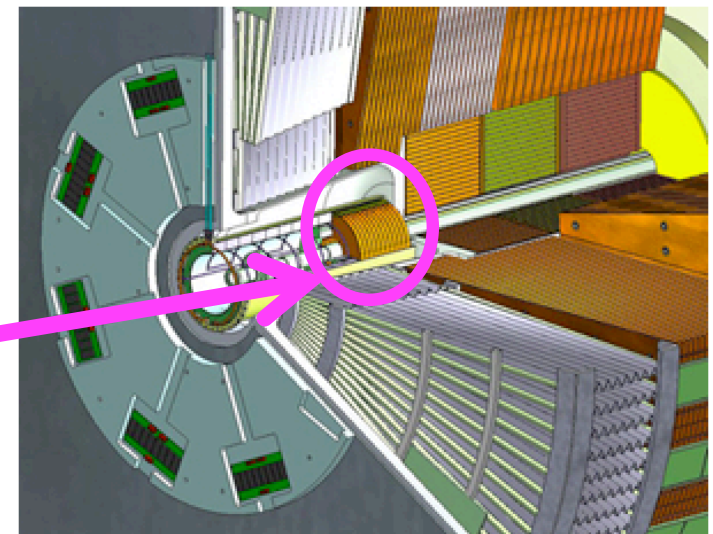
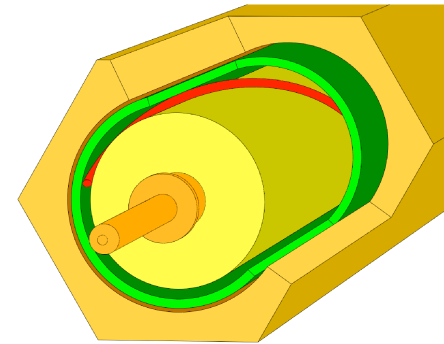
- **HEC cold electronics do not need to be replaced, so there is no need to remove the large cold cover (means FCal summing boards not accessible)**





Forward Calorimeter

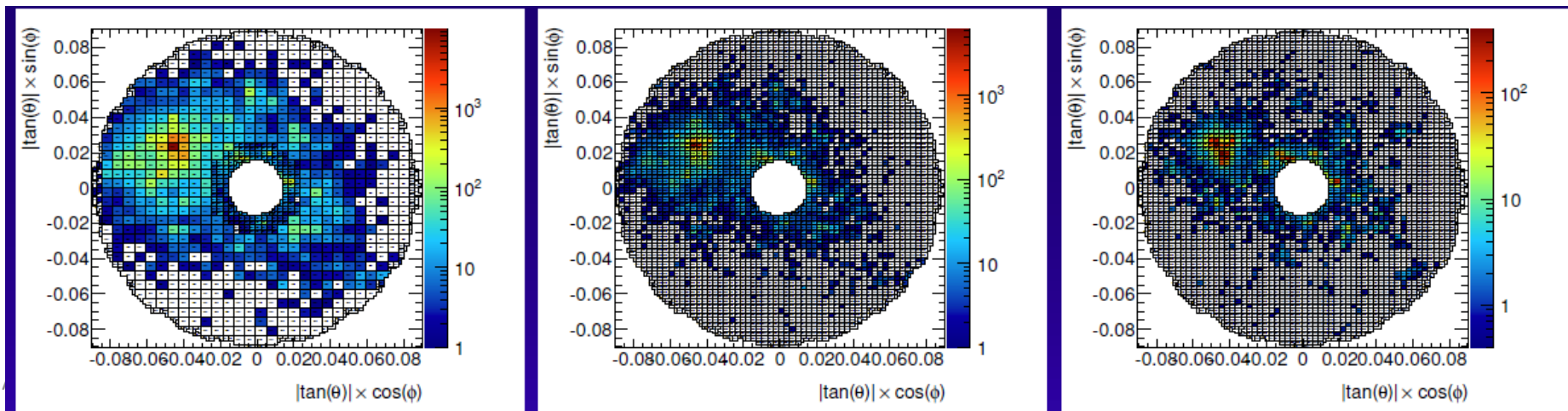
- ❖ ATLAS EM and hadronic calorimeter detectors are able to cope with HL-LHC conditions
- ❖ Only exception is ATLAS FCAL, which uses novel (US) design with absorber rods housed in absorber lattice, and small LAr gaps (270 – 500 μm)
- ❖ Beyond design luminosity, enormous rates lead to space charge problems (even possibly boiling of LAr), as well as voltage drops across HV resistors
 - Utilizing the same design concept but with thinner gaps (down to 100 μm), one could tolerate the HL-LHC conditions
 - Using this technique, solutions being investigated include:
 - A new calorimeter (“sFCAL”), or
 - A “Mini-FCAL”
(placed in front of the existing FCAL)





FCAL (cont'd)

- ❖ Recent simulations suggest LAr will not boil (though margin is small)
 - However, geometry is complicated and difficult to simulate accurately
 - A mockup has been built, but testing is so far inconclusive
 - Further LAr sub-cooling by $\Delta T = -1.6$ K successfully tested during shutdown and $\Delta T = -2$ K is believed to be possible
- ❖ FCAL performance issues have been taken up by high-eta task force
 - Gets tied in with fwd tracking, possible new “preshower-type” detector in space previously occupied by MBTS, etc.
 - Suggestion has also been made to increase readout granularity in case of sFCAL (probably only in EM-compartment, sFCAL1)





FCAL Decision

❖ Decision of final approach still to be made

- Originally scheduled for March 2015, pushed back to at least June 2015, and perhaps to end 2015 (any later would jeopardize readiness of sFCAL by Feb. 2023, when it is needed for installation assuming current LHC schedule)
- Continuing to try progress on multiple fronts, to prepare decision:
 - Finalize understanding of whether LAr boiling will occur if no change is made in the forward region
 - Explore performance, and associated physics impact, of various scenarios (degraded FCAL, sFCAL with low/high granularity, miniFCAL), both standalone and as part of large eta task force
 - Very limited mpwr, plus not very mature simulation framework, ...
 - Work to solve engineering issues related to realization of miniFCAL concept

❖ Until final decision, need to carry options

- If LAr miniFCal is chosen, US will seek to join the construction project



Readout Electronics



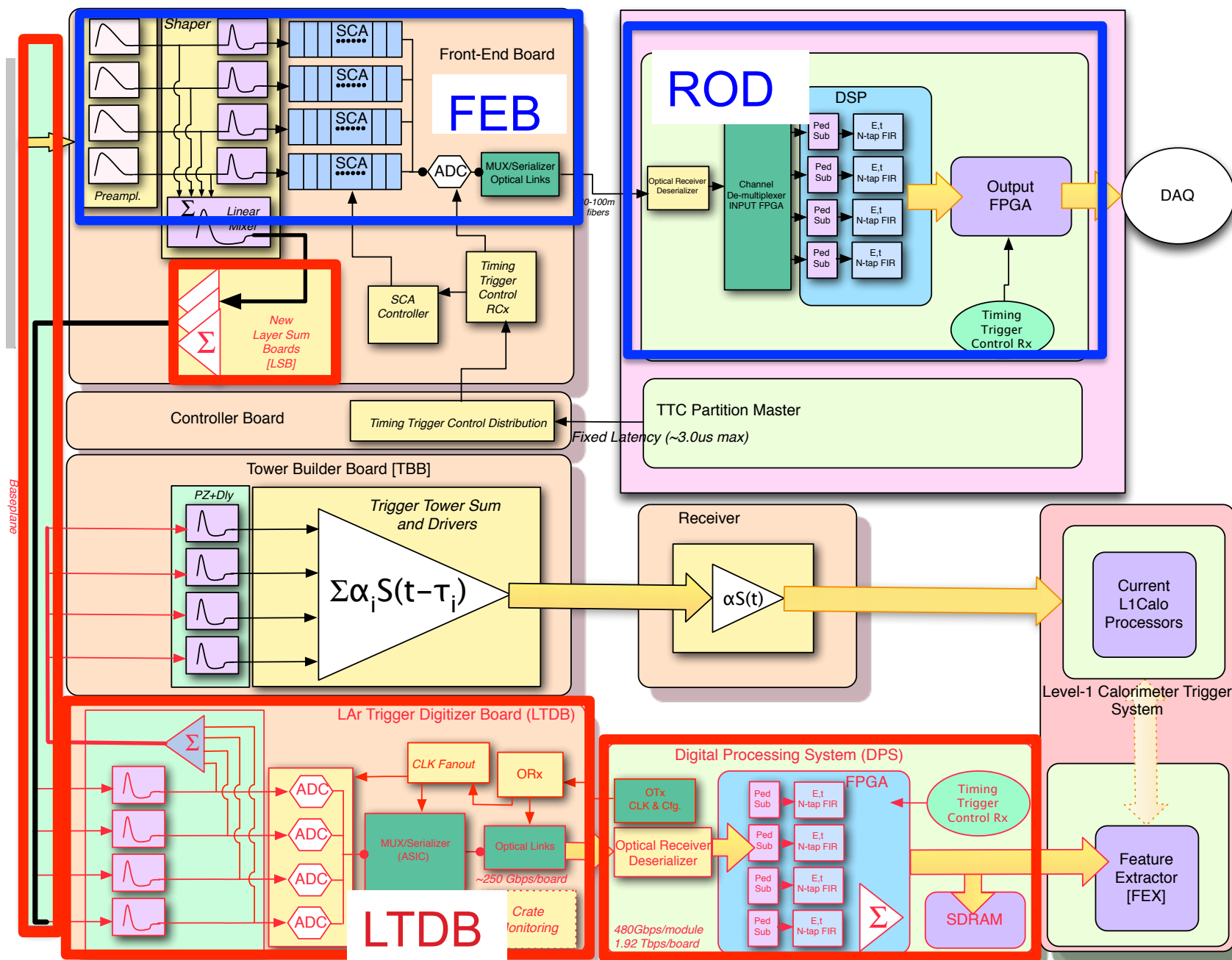
New LAr Readout Electronics

- ❖ To adapt to HL-LHC TDAQ architecture, need to replace LAr readout
 - Current readout would continue to limit L1 rate to 100 kHz, and latency to $\sim 2.5 \mu\text{s}$

- ❖ Plan to develop new “FEB2”, digitizing and sending off detector all channels at 40 MHz
 - Move pipeline off detector, out of radiation environment
 - Have full granularity calo. info available for new L1 trigger, so that shower shape info, etc. can be used to allow EM trigger thresholds to remain low

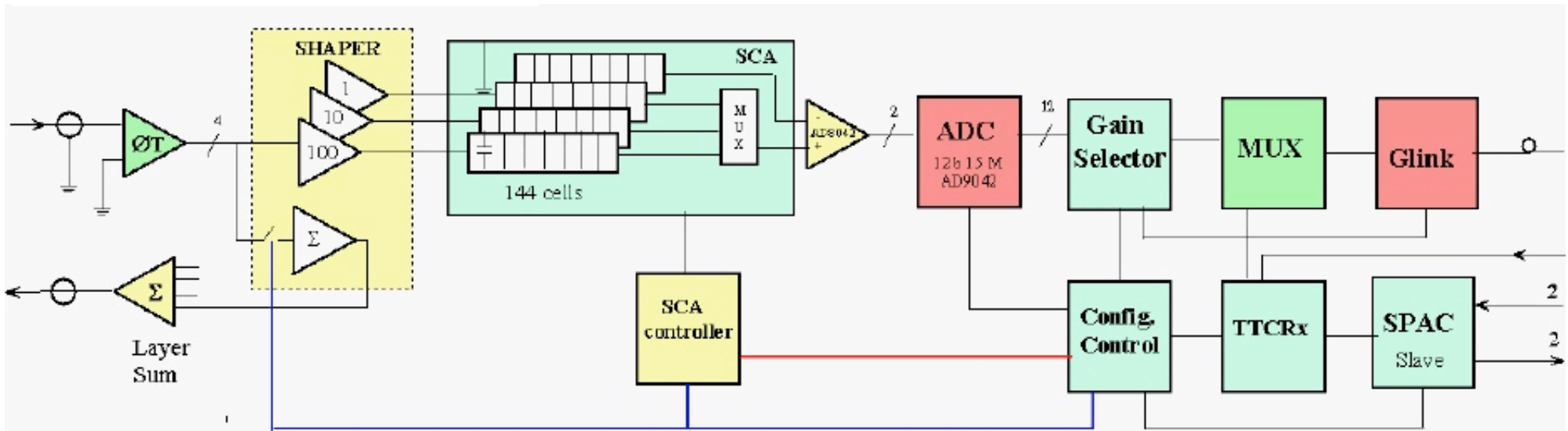
(use Phase 1 trigger upgrade electronics as part of new L0 trigger used to see L1 track trigger)

- ❖ Will need new backend electronics (“ROD2”) to receive and process the FEB2 data (boundaries between LAr and TDAQ become more blurry, certainly for L1)



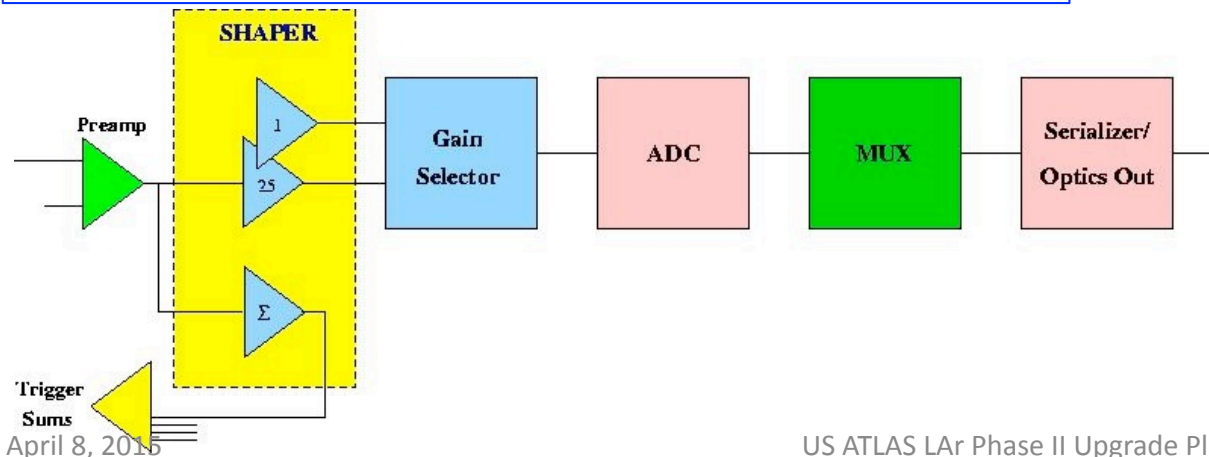
Red for phase-1. Blue for phase-2.
US efforts are mostly in the front-end.

The front-end:



Current detector readout scheme on the (US-designed) FEB

Proposed readout upgrade (FEB2)



Critical R&D:

1. Pre-amp + Shaper
2. ADC (12 to 16 bit)
3. Optical Link (10 G)



FE Electronics Developments

- ❖ Working to consolidate US efforts, with a main goal being the investigation of the potential of 65 nm CMOS to meet our various (and varied) needs for FEB2 ASICs:
 - Preamp/shaper ASIC
 - Prototyped originally in SiGe (UPenn/BNL)
 - New BNL effort on 65 nm CMOS, with major challenge being 16-bit dynamic range
 - By fall, expect UPenn to shift focus to help with 65 nm investigation
 - ADC
 - 130 nm ADC (pipeline + SAR) developed at Columbia is nearing production phase for use in Phase I, and design effort turning to 65 nm for Phase II
 - UT Dallas effort focusing on (all-SAR version of) 65 nm design
 - Groups have agreed to collaborate, and JP and Columbia engineer are going to UTD next week to explore further how best to proceed
 - Optical links
 - Need ~100 Gpbs of rad-tol optical link bandwidth per 128-channel FEB2
 - SMU working on serializer/driver for ~ 10 Gbps optical link, as well as optical components (as part of Versatile Link project)
- ❖ In ~1 year, should have enough experience (and even first prototypes) to gauge potential to use 65 nm as a common technology for the various blocks
 - Later step would evaluate whether further ASIC consolidation would be possible/desirable



Project Management



US Phase-II Deliverables

- ❖ WBS 6.3.6 - New Forward Calorimeter (sFCAL)
 - 2 EM modules (4 Hadronic modules (from Canada, MPI, ...?))
 - Cold electronics (HV distribution and summing – all passive)
- ❖ WBS 6.3.7 - Frontend (on detector) electronics components
 - Preamp/shaper, ADC, gain selector, serializer, optical Links
- ❖ WBS 6.3.8 – Frontend Board (FEB2) system integration
 - FEB2 design, including control, clock distribution, LV power, cooling, ...
- ❖ US interest and possible roles in the BE Electronics are still being fleshed out.

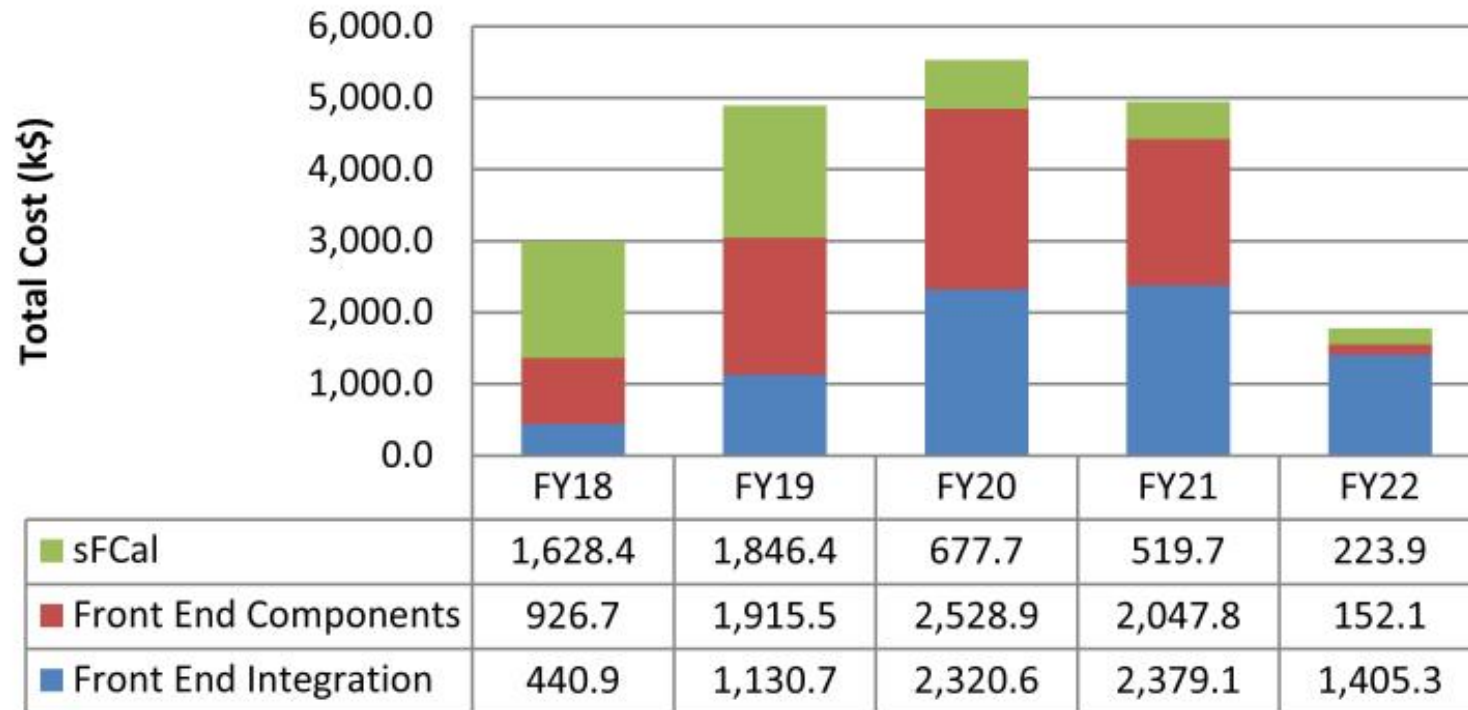


US LAr Institutions

- ❖ WBS 6.3.6 - sFCAL: U of Arizona
- ❖ WBS 6.3.7 - Frontend Electronics Components:
Brookhaven, Columbia, U of Penn, SMU
- ❖ WBS 6.3.8 – Frontend System Integration (FEB):
Brookhaven, Columbia
- ❖ Backend Electronics:
U of Arizona, U of Oregon, Stony Brook University,
Brookhaven (also, new expression of interest from MSU)
- ❖ U of Iowa has been participating in LAr for some time already,
and also has interest in Phase II – still being discussed



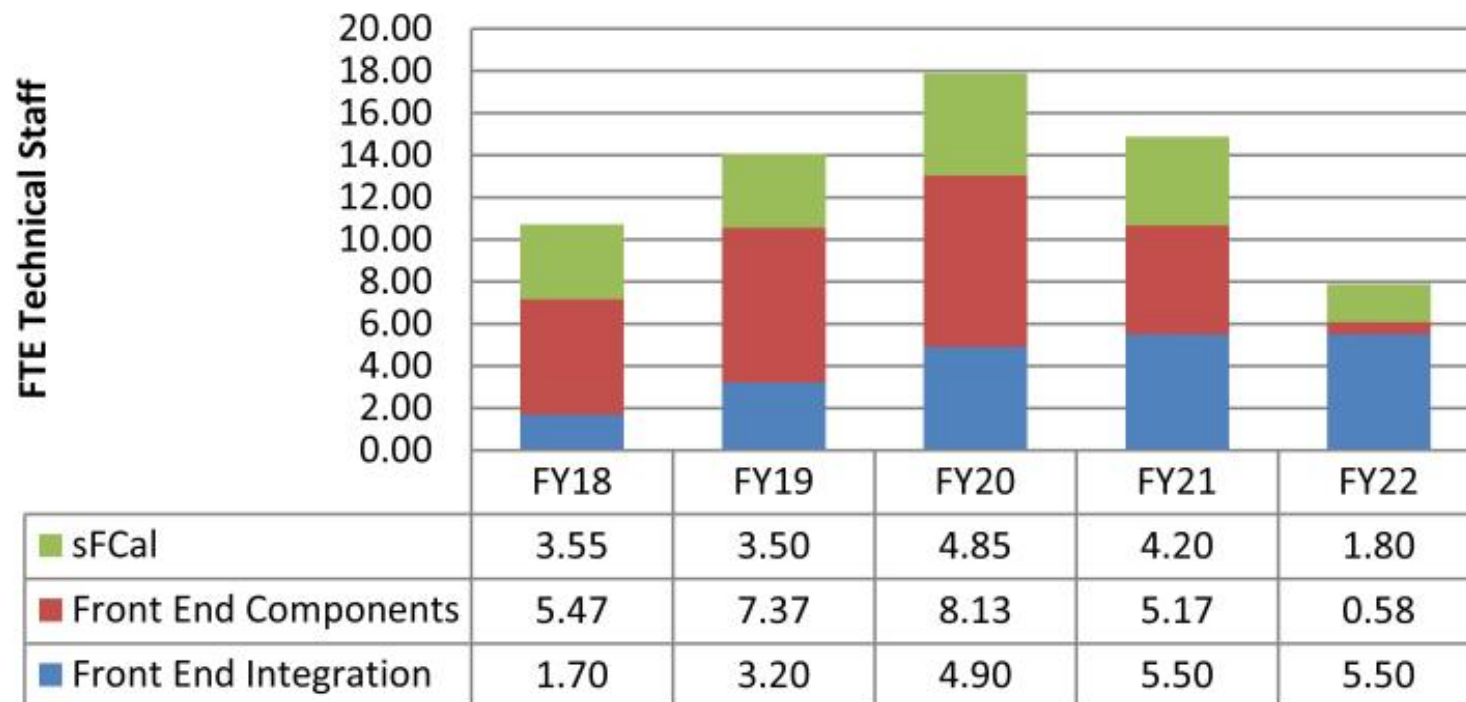
US LAr Phase 2 Construction Total Cost



Item	Cost (k\$)
sFCal	4,896
Front End Components	7,571
Front End Integration	7,677
Total	20,144



US LAr Phase 2 FTE Technical Staff



Item	Tech FTE
sFCal	17.9
Front End Components	26.7
Front End Integration	20.8
Total	65.4



Summary

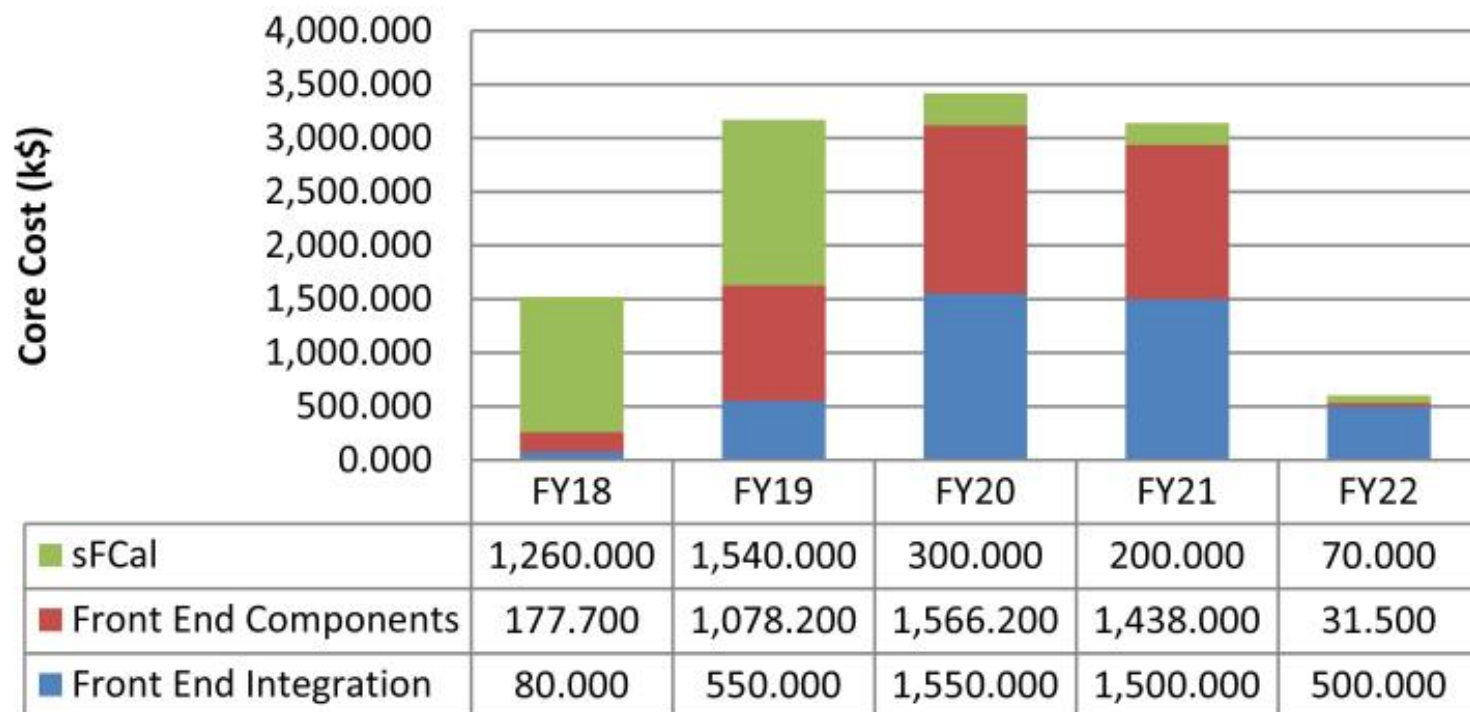
- ❖ US ATLAS plays many critical roles in LAr Phase-II Upgrade.
- ❖ FCAL upgrade option will be finalized in 2015. US plans to contribute in either sFCAL or miniFCAL scenarios.
- ❖ Readout upgrade concentrates on FEB2 and US is leading the efforts. Current R&D centered on FE components and options that will influence the system integration. Decisions in the R&D course will guide the efforts to construction.
- ❖ There is also considerable US interest and expertise in the BE electronics. Discussions concerning BE responsibilities are less advanced so far (and will involve also TDAQ/LAr boundaries).
- ❖ First bottom-up estimate for construction, 0th order. A lot of work will be needed to finalize the budget.



Backup Slides



US LAr Phase 2 Construction Core (k\$)

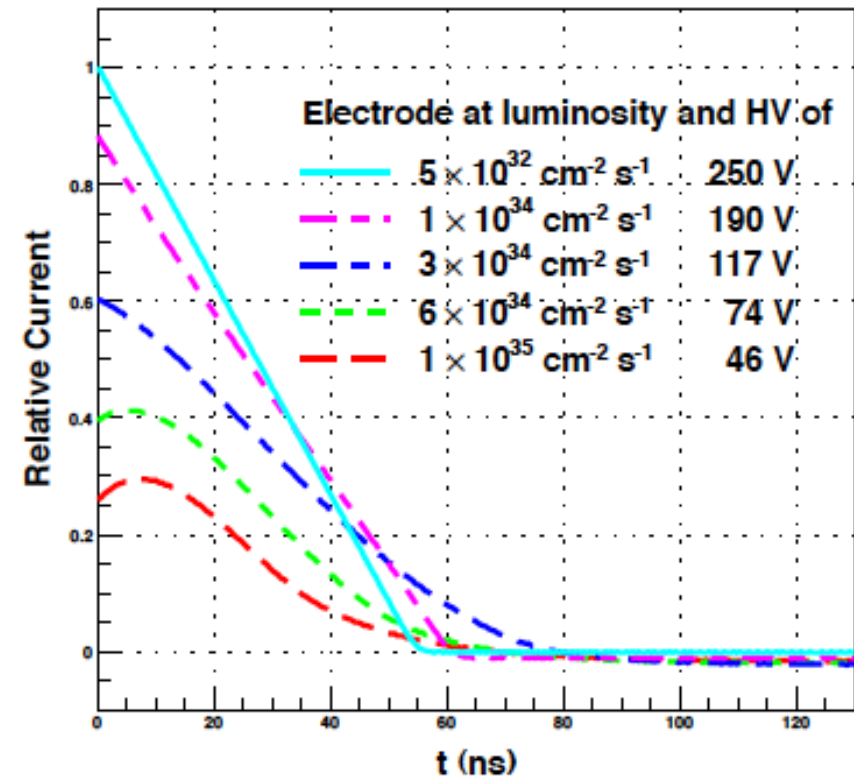


Item	Core Cost (k\$)
sFCal	4,180
Front End Components	4,292
Front End Integration	3,370
Total	11,842

ATLAS LAr CORE (kCHF)		US %
Base	32,124	32.1%
Option	15,096	
Total	47,220	21.8%

Degradation in FCAL Response vs Lumi

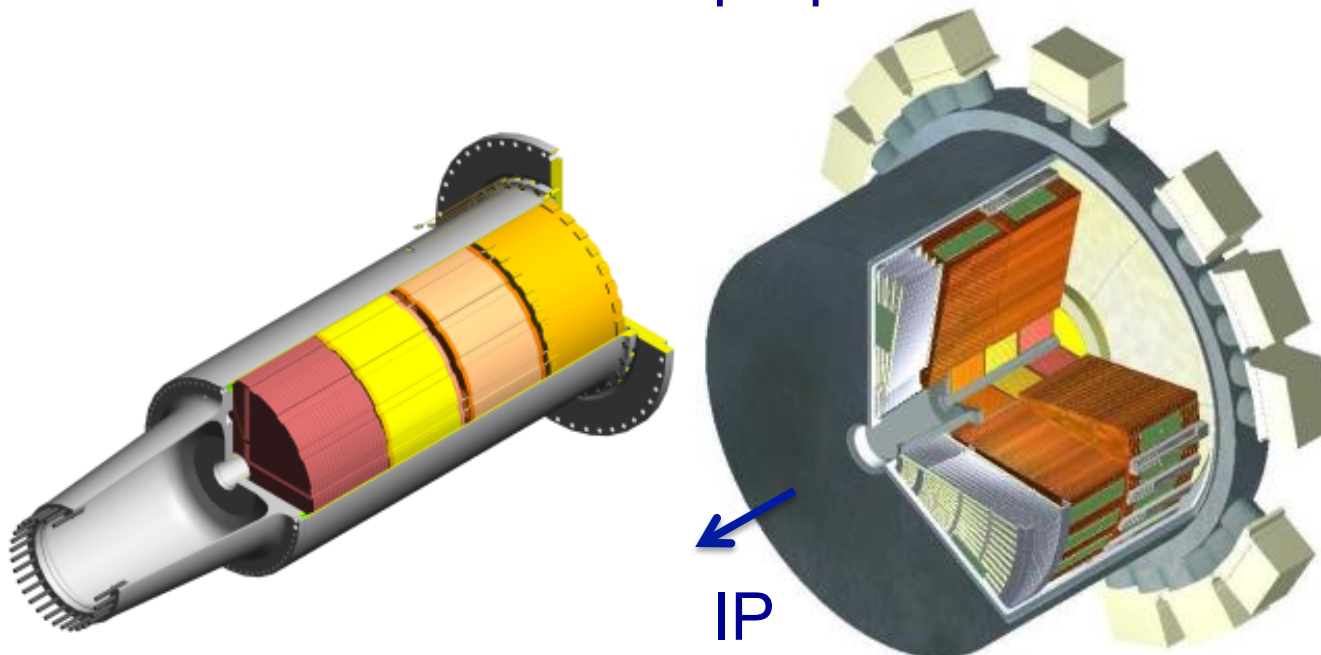
Figure 3.4: Simulated signal pulses at $\eta = 4.7$ for different luminosities, assuming a constant rate from minimum bias background. For each luminosity the same signal energy is deposited in the FCal1 module on top of the minimum bias background and the signal pulse is extracted. For luminosities below $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ the signal on the electrodes is the familiar triangular pulse. At higher luminosities both the magnitude and shape of the pulse are degraded.



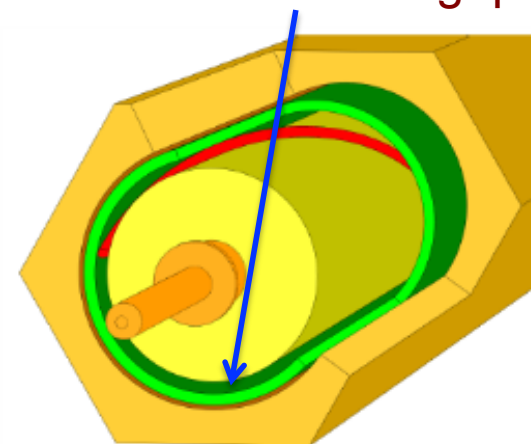
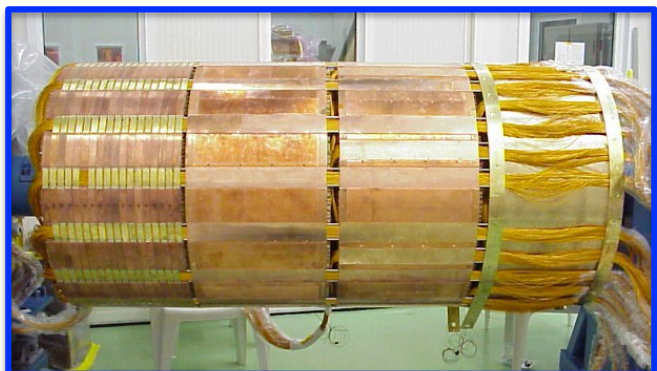


sFCal is like the FCal

The FCal and the US proposed sFCal.



sFCal has narrower LAr gaps





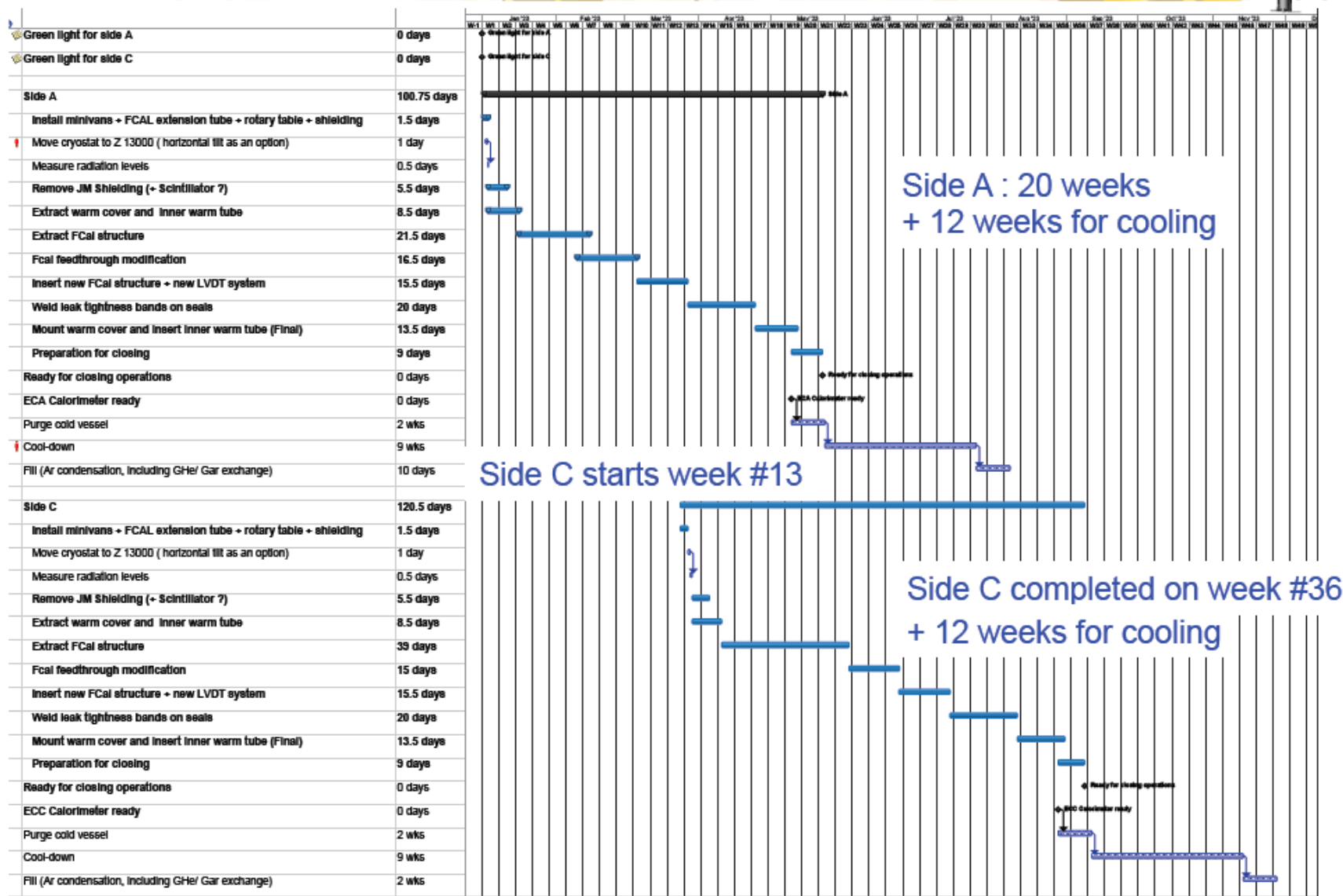
... but the sFCal differs in key features

- ❖ Has smaller ionization gaps to push the space-charge threshold out of reach
- ❖ Has smaller values for the HV protection resistors in the HV distribution system to keep the HV across the gaps at the nominal value
- ❖ Has local cooling to prevent boiling the liquid argon

Increased sFCal readout granularity

- Most logical way to increase the granularity would be to remove the signal summing (for summed channels).
- Having ONLY unsummed channels in the sFCal1 would yield 3065 FCal1 channels instead of the current 1008:
 - This would require 24 FEBs (assuming 128 channels / FEB) for the FCal1 and $24+4+2 = 30$ in total (assuming no changes to the FCal2 or FCal3 granularities). So 16 additional FEBs.
[N.B. I had these numbers wrong in a previous version of this talk]
 - Can 16 FEBs be installed in existing empty half-crate? There are 19 slots.
- Need to remember that the additional signals also need to get to the Front-End crate. Need a cable route and a feedthrough of some sort.

Installation time schedule



sFCal Production schedule



Main milestones of the last sFCal production schedule (Sept. 2012)

sFCal R&D : Sept. 2011 – Feb. 2014

sFCal approval : Beginning 2015

sFCal1 production : Jan. 2015 → Apr. 2020

sFCal2 production : Nov. 2015 → Feb. 2020

sFCal3 production : Jan. 2016 → Oct. 2019

sFCal-A integration (at Cern) : Jan. 2018 → March 2020

sFCal-A beam calibration : May 2020 → Aug. 2020

sFCal-C integration (at Cern) : Jul. 2019 → May 2021

sFCal-C beam calibration : May 2021 → Aug. 2021

Preparation for installation : Sept. 2021 → Dec. 2021

sFCal ready for installation in the cryostat (both) : **Beg. 2022**

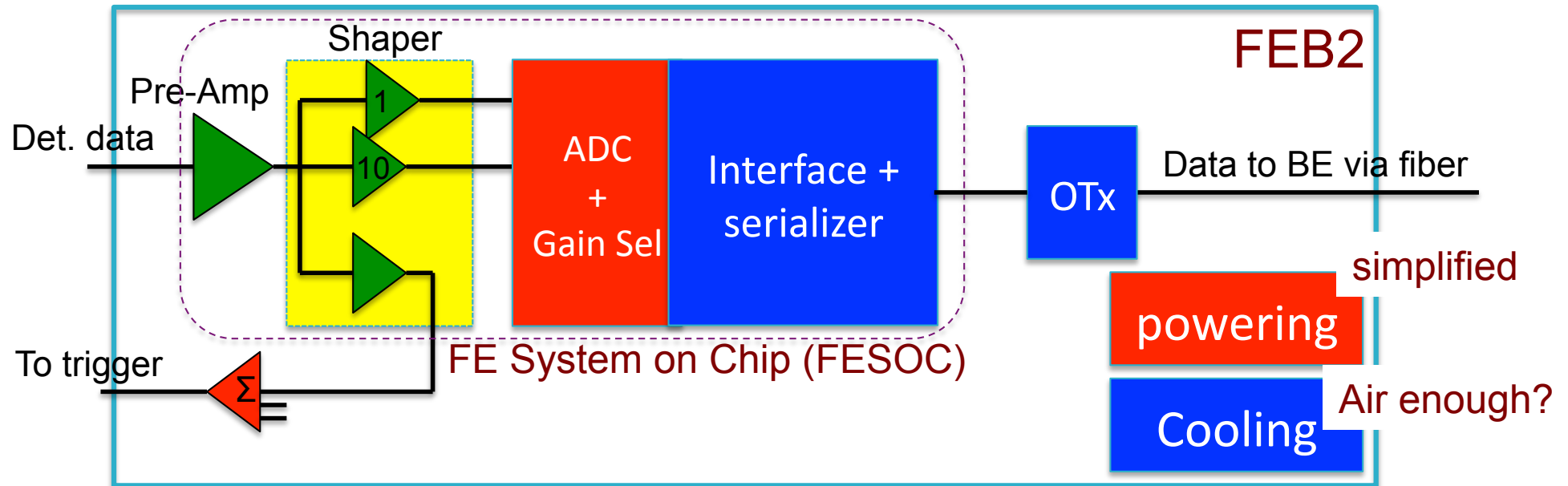
Will High Granularity sFCal
need more production time ?

Some optimization
is possible here for
contingencies

Providing the production can really start just after the approval, a decision by end of 2015 is still consistent with a status “ready for installation” by beg. 2023
but very close to be critical

FE System-on-Chip

The idea has been around awhile but now it's a proposal



- FESOC, a one die or two die chip that integrates the three key ASICs. By combining the ADC with the serializer (both in 65 nm CMOS), one eliminates the output circuits for the ADC hence saves power.
- Impact on system integration and in construction:
 - Simplified FEB2, powering and possibly air (not water) cooling.
 - Reduce production cost in chip packaging and QA, and in FEB PCB.
 - The impact on yield may be small as the yield of 65 nm CMOS is expected to be high and the cost of die is small.